JNTUA COLLEGE OF ENGINEERING (Autonomous), ANANTHAPURAMU
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
COURSE STRUCTURE
***M.TECH (Regular)* - Digital Systems and Computer Electronics (DSCE)**
(w.e.f 2015-16 Admitted Batch)

M.Tech I Semester

S.No	Subject Code	Subject	Theory	Lab	Credits
1.	15D41101	Structural Digital System Design	4	-	4
2.	15D41102	Advanced Computer Networks	4	-	4
3.	15D41103	Advanced Computer Architecture	4	-	4
4.	15D41104	System Design using Microcontrollers	4	-	4
5.	15D41105 15D41106 15D41107 15D41108	Elective-I a. Advanced Operating Systems b. Network Security and Cryptography c. Electronic Design Automation Tools d. Quality and Reliability	4	-	4
6.	15D41109 15D41110 15D42102 15D41111	Elective-II a. Nano Electronics b. CMOS VLSI Design c. Advanced Digital Signal processing d. Cloud Computing	4	-	4
7.	15D41112	Structural Digital System Design Lab	-	3	2
Contact periods/week			**24**	**03**	**26**
			Total/week	**27**	

M.Tech II Semester

S.No	Subject Code	Subject	Theory	Lab	Credits
1.	15D41201	Embedded System Design	4	-	4
2.	15D41202	Image & Video Processing	4	-	4
3.	15D41203	ADSP Architectures	4	-	4
4.	15D41204	ASIC Design	4	-	4
5.	15D41205 15D41206 15D41207 15D41208	Elective-III a. Low Power VLSI Design b. CPLD & FPGA Architectures and Applications c. Hardware Software Co Design d. Big Data	4	-	4
6.	15D41209 15D41210 15D41211 15D41212	Elective-IV a. Fuzzy Systems and Neural Networks b. MEMS and its Applications c. Testing and Testability d. Wireless Sensor Networks	4	-	4
7.	15D54201	Research Methodology (Audit Course)	2	-	-
8.	15D41213	Embedded Systems Lab	-	3	2
Contact periods/week			**26**	**03**	**26**
			Total/Week	**29**	

M.Tech III & IV SEMESTERS

Code	Name of the Subject	T	P	C
15D41301	**III Semester** Seminar- I	0	4	2
15D41401	**IV Semester** Seminar- II	0	4	2
15D41302	**III & IV Semester** PROJECT WORK	--	--	44
	Total	**24**	**8**	**48**

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D41101) STRUCTURED DIGITAL SYSTEM DESIGN

Course Objective:

- To study about structural functionality of different Digital blocks (Both combinational and Sequential)
- To provide an exposure to ASM charts, their notations and their realizations.
- To provide an exposure to VHDL and different styles of modelling using VHDL.
- To introduce concept of micro programming and study issues related to micro programming

Course Outcome:

After Completion of this course students will be able to

- Understand structural functionality of different digital blocks
- Represent and Realize their designs in ASM charts
- Represent their designs in different modelling styles by using VHDL
- Understand concept of Micro program and issues related to micro programming

UNIT-1

BUILDING BLOCKS FOR DIGITAL DESIGN: Multiplexer, Demultiplexer, Decoder, Encoder, Comparator, Adder, ALU, Carry-look-ahead adder.

BUILDING BLOCKS WITH MEMORY: Clocked building blocks, register building blocks, RAM, ROM, PLA, PAL, Timing devices.

UNIT -II

DESIGN METHODS: Elements of design style, top-down design, separation of controller and architecture, refining architecture, and control algorithm, Algorithmic State Machines, ASM chart notations.

UNIT-III

REALISING ASMS - Traditional synthesis from ASM chart, multiplexer controller method, one-shot method, ROM based method.

ASYNCHRONOUS INPUTS AND RACES - Asynchronous ASMs, Design for testability, test vectors, fault analysis tools.

UNIT-IV

MICROPROGRAM AND DESIGN: Microprogramming, Microprogramme sequencer 2910, designing microprogrammed computer. Power distribution noise, cross talk, reflections, line drivers and receivers.

UNIT-V

MODELLING WITH VHDL: CAD tools, simulators, schematic entry, synthesis from VHDL.

DESIGN CASE STUDIES: Single pulser, system clock, serial to parallel data conversion, traffic light controller.

Text Books:

1. Prosser and Winkel, "The Art of Digital Design", Prentice Hall.
2. Roth, “Digital System Design using VHDL”, Mc. Graw Hill, 2000

References:

1. William Fletcher, An Engineering Approach to Digital Design, 1st Edition, Prentice-Hall India, 1997.
2. William J Dally and John W Poulton, Digital Systems Engineering, Cambridge University Press, 2008.
3. Jayaram Bhasker, A VHDL Primer, 3rd edition, Prentice-Hall India, 2009.
4. J. Bhasker; A VHDL Primer, Addison - Wesley.
5. VHDL for Programmable Logic - Kevin Skahill, Cypress Semiconductors

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(15D41102) ADVANCED COMPUTER NETWORKS

Course Objective:

- To study about different protocols related to advanced computer networks such as wireless lans Wimax and so on.
- To study about security features associated with different advanced computer networks.

Course Outcome:

After completion of this course students will be able to

- Know the functioning different protocols associated with modern computer network system
- Know the security features associated with modern computer network system.

UNIT-I

Review of data communication standards, topologies, OSI, TCP/IP models , Transmission media, circuit switched networks, packet switched networks, Point to Point Protocol (PPP),Asymmetric Digital Subscriber Line (ADSL)

UNIT-II

Fast Ethernet, Gigabit Ethernet, Wireless LANs, Bluetooth, WiMax, Virtual LANs,

UNIT-III

Advanced Network Architectures -SONET/SDH, Frame Relay and ATM architectures and services, VPN architectures, IP over ATM, MPLS, RSVP

UNIT-IV

IPv6 protocol, Socket interface, Domain Name System, Simple Mail Transfer Protocol, WWW and HTTP, Simple Network Management Protocol

UNIT-V

Voice Over IP, Cryptography, Network security, Digital Signatures, IPSec, Firewalls,

Text Books :

1. BEHROUZ A. FOROUZAN, "Data Communications and Networking", 4th Ed, Tata McGraw-Hill, New Delhi, 2006
2. LEON-GARCIA, INDRA WIDJAJA, "Communication Networks – Fundamental concepts and Key architectures", TMH, 2000

References:

1. Jim Kurose, Keith Ross, "Addison *Computer Networking: A Top Down Approach",* 4th edition, Wesley, July 2007.
2. Andrew S. Tanenbaum "Computer Networks", 4th Edition, Pearson Education, 2008
3. William Stallings, "Data and Computer Communication", 9th edition, Prentice hall, 2010

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(15D41103) ADVANCED COMPUTER ARCHITECTURE

Course objective:

- To study about various parallel computer models and also to study the program and network properties
- To study the concepts of pipelining and super scalar techniques.
- To study about architectures of multi processors and multi computers

Course ***Outcome:***

After completion of the course the students will be able to

- Know about different parallel computer models and their network properties.
- Understand about different concepts related to pipelining and super scalar techniques.
- Get complete knowledge regarding multi processors and multi computers.

UNIT - I

Parallel Computer Models – System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

UNIT - II

Program and Network Properties- Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

UNIT-III

Processors and Memory Hierarchy- Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations

UNIT - IV

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

NIT- V

Multiprocessors and Multicomputers Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

Text Books:

1. Hwang kai, "Advanced Computer Architecture", McGraw-Hill, 2001.
2. Patterson, David and Hennessy John**,** Morgn Kaufmann, "Computer Architecture",2001.

References:

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennesey, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition PrenticeHall India, 2009.

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(15D41104) SYSTEM DESIGN USING MICROCONTROLLERS

Course Objective:

- To get knowledge in system design using Micro controllers
- To Study the architectural features and and programming aspects of ARM controllers/processors.
- To learn about memory management in the system design applications

Course Outcome:

After completion of this course students will be able to

- Gets complete knowledge about the system design concepts using Micro controllers.
- Understand thoroughly the architectural and programming concepts of ARM controllers.
- Know about the memory management concepts in system design.

UNIT-I: ARM Architecture

ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT-II: ARM Programming Model-I

Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III: ARM Programming Model-II

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT-IV : ARM Programming

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT-V: Memory Management

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

Text Books:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guides- Designing & Optimizing System Software", 2008, Elsevier.
2. Jonathan W. Valvano – Brookes / Cole, 1999, "Embedded Microcomputer Systems, Real Time Interfacing", Thomas Learning.

References:

1. Intel and ARM Data Books on Microcontrollers.
2. Embedded System Design-Frank Vahid/Tony Givargis, John Willey, 2005.
3. Microcontroller (Theory and Applications) Ajay V Deshmukh, Tata McGraw-Hill, 2005.
4. An Embedded Software Primer-David E.Simon, Pearson Education, 1999.

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(15D41105) ADVANCED OPERATING SYSTEMS

Course Objective:

- To Study in detail about kernel structures associated with various Operating systems
- To Study in detail about various systems calls, statements and their arguments associated with Unix .
- To Study in detail about various systems calls, statements and their arguments associated with Linux .

Course Outcome:

After completion of the course students will be able to

- Get complete knowledge regarding different types of operating systems and their Kernel structures.
- To work effectively on Unix Platform
- To work effectively on Linux Platform

UNIT I

INTRODUCTION

General Overview of the System: History – System structure – User perspective – Operating system services – Assumptions about hardware. Introduction to the Kernel: Architecture of the UNIX operating system – Introduction to system concepts. The Buffer Cache: Buffer headers – Structure of the buffer pool – Scenarios for retrieval of a buffer – Reading and writing disk blocks – Advantages and disadvantages of the buffer cache.

UNIT II

UNIX I*:* Overview of UNIX system, Structure, files systems, type of file, ordinary & Special files, file permissions, Introduction to shell. UNIX basic commands & command arguments, Standard input / output Input / output redirection, filters and editors, System calls related file structures, input / output process creation & termination.

UNIT III

INTERPROCESS COMMUNICATION IN UNIX: Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Speces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT IV

INTRODUCTION TO NETWORKS AND NETWORK PROGRAMMING IN UNIX: Network Primer, TCP/IP, Internet Protocols, Socket Programming, Introduction & overview, UNIX domain protocols, Socket Addresses, Elementary Socket system calls, Simple examples.

UNIT V

LINUX: Introduction to LINUX System, Editors and Utilities, Type of Shells, Shell Operations, File structure, File Management, Operations. Memory Management Policies: Swapping – Demand paging. The I/O Subsystem: Driver Interface – Disk Drivers – Terminal Drivers– Streams – Inter process communication.

Text Books:

1. Maurice J.Bach, “The design of the UNIX Operating Systems”, PHI
2. Kernighan & Pike, “The UNIX Programming Environment”, PHI

References:

1. W.Richard Stevens, “UNIX Network Programming”, PHI, 1998.
2. Richard Peterson, “The Complete reference LINUX”, TMH
3. Ritchie & Yates, “UNIX User Guide”.

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(15D41106) NETWORK SECURITY & CRYPTOGRAPHY

Course Objective:

- To study about need and role of security and cryptography in computer networks.
- To study about different techniques associated with encryption.
- To study about different algorithms associated with computer networks.
- To study about different security architecture and designing issues related to fire walls.

Course Outcome:

After completion of this course students will be able to know

- The need and role of security and cryptography in computer networks.
- Gain knowledge about different techniques associated with encryption.
- Functioning of different algorithms associated with computer networks.
- Gain knowledge regarding different security architecture and designing issues related to fire walls.

UNIT – I

Introduction: Attacks, services and mechanisms, security attacks, security services, a model for internet work security, protection through cryptography, the role of cryptography in network security.

UNIT – II

Conventional Encryption: Substitution techniques and transposition techniques, block cipher principles, block cipher design principles, block cipher modes of operation. The data encryption standard

UNIT – III

Public-key encryption: Principles of public-key cryptosystems, the RSA algorithm, key management. Authentication requirements, authentication functions, message authentication codes, hash functions.

UNIT – IV

Digital Signatures and Authentication Protocols: Digital signatures, Digital signature standard, Authentication Protocols, MD5, message digest algorithm, secure hash algorithm, HMAC.

UNIT – V

Mall security & IP security: Pretty good privacy, IP security overview, IP security architecture, Intruders, viruses and related threats, firewall design principles

Text Books:

1. W. Stallings**, "**Cryptography & Network Security", 3/e, PHI, 2003
2. Eric Maiwald**, "**Fundamental of Network Security", Dreamtech press Osborne MGH, 2004

References:

1. Sean Convery, " Network Security Architectures, Published by Cisco Press, First Ed. 2004.
2. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
3. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
4. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
5. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3rd Edition, Pearson Education, 2003.
6. Jeff Crume, "Inside Internet Security" Addison Wesley, 2005.

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(15D41107) ELECTRONIC DESIGN AUTOMATION TOOLS

Course Objective:

- To provide exposure to different types of synthesis and synthesis tools
- To study about mixed signal design
- To study about design of PCB and different tools that are employed in design of PCB

Course Outcome:

After completion of the course the student will be able to

- Perform various types of simulation using different simulating tools.
- Get complete knowledge regarding mixed signal design
- Design high speed PCB using simulation and layout tools

UNIT-I: Synthesis and Simulation using HDLs

Verilog and logic synthesis, VHDL and logic synthesis, memory synthesis, FSM synthesis, Performance-driven synthesis, Simulation-types of simulation, logic systems, working of logic simulation, cell models, delay models, static timing analysis, formal verification, switch-level simulation, transistor-level simulation, CAD tools for synthesis and simulation Modelsim and Leonardo Spectrum

UNIT-II: Circuit design and Simulation using Pspice

Pspice models for transistors, A/D & D/A converters, sample and hold circuits, digital system building blocks, design and analysis of analog and digital circuits Using Pspice.

UNIT-III: Mixed Signal Design

Fundamentals of analog and digital simulation, mixed signal simulator configurations, understanding modeling, integration to CAD environments, analysis of analog circuits-A/D and D/A converters, up and down converters, comparators etc.

UNIT-IV: PCB Design and Layout

An overview of high speed PCB design, design entry, simulation and layout tools for PCB, introduction to Orcad PCB Design Tools.

UNIT-V: Electronic Instrument Design

Electronic circuit design, circuit layout, necessary software, debugging and testing, case studies offering practical electronic instrument design.

Text Books:

1. J.Bhaskar, “A Verilog HDL Synthesis”, BS Publications.
2. M.H.Rashid, “SPICE for circuits and electronics Using Pspice”, Prentice Hall, Second Edition.
3. Kim R.Fowler, “Electronic Instrument Design”, Oxford University press.

References:

1. J.Bhaskar, “A VHDL Synthesis Primer”, B S Publications.
2. M.J.S.Smith, “Application-Specific Integrated Circuits”, Wesley
3. Orcad, “ORCAD-Technical reference manual”, USA.
4. Analogy Nic, “SABER- Technical reference manual”, USA.

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	4	**0**	**4**

(15D41108) QUALITY & RELIABILITY

Course Outcomes : After completion of this subject, students will be able to

- Design any system or component or circuit with high reliability.
- Analyze reasons for the failures of circuits or systems and provide necessary repair for reliable functioning of those systems.
- Provide relevant mechanisms for proper availability and maintainability of the systems.

UNIT-I:

Elements of probability theory Probability distributions: Random variables, density and distribution functions. Mathematical expectation. Binominal distribution, Poisson distribution, normal distribution, exponential distribution, Weibull distribution. Reliability: Definition of Reliability. Significance of the terms appearing in the definition. Component reliability, Hazard rate, derivation of the reliability functions in terms of the hazard rate. Hazard models.

UNIT-II:

Failures: Causes of failures, types of failures (early failures, chance failures and wear-out failures). Modes of failure. Bath tub curve. Effect of preventive maintenance. Measures of reliability: mean time to failure (MTTF) and mean time between failures (MTBF).

UNIT-III:

Reliability logic diagrams: (reliability block diagrams) Classification of engineering systems: series, parallel, series-parallel, parallel-series and non-series-parallel configurations (mainly for Electronic system configurations). Expressions for the reliability of the basic (Electronic systems) configurations.

UNIT-IV:

Reliability evaluation of Non-series-parallel configurations (mainly for Electronic systems configurations): minimal tie-set, minimal cut-set and decomposition methods. Deduction of the minimal cutsets from the minimal path sets. More than two components Electronics systems reliability evaluation: Series systems, parallel systems with two and more than two components, Network reduction techniques. Minimal cutest / failure mode approach.

UNIT-V:

Discrete Markov Chains: General modelling concepts, stochastic transitional probability matrix, time dependent probability evaluation and limiting state probability evaluation, absorbing states (mainly for Electronic systems). Continuous Markov Processes: Modelling concepts, State space diagrams, Stochastic Transitional Probability Matrix, Evaluating limiting state Probabilities. Reliability evaluation of repairable systems (mainly for Electronic systems).

Text Book:

1. Reliability Evaluation of Engineering Systems", Roy Billinton and Ronald N Allan, Plenum Press.

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(15D41109) NANO ELECTRONICS

Course Objective:

- To study about different quantum devices
- To study in detail about nano devices and nano architectures and their computations
- To study about Molecular nano Electronics

Course Outcome:

After completion of the course the student will be able to

- Gain complete knowledge regarding different Quantum Devices.
- Know about nano devices and nano architectures and their computations.
- Know about Molecular Nano Electronics

UNIT – I: Quantum Devices:

Charge and spin in single quantum dots- Coulomb blockade – Electrons in mesoscopic structures - single electron transfer devices (SETs) – Electron spin transistor – resonant tunnel diodes, tunnel FETs - quantum interference transistors (QUITs) - quantum dot cellular automata (QCAs) - quantum bits (qubits).

UNIT – II: NanoElectronic Devices:

Electronic transport in 1,2 and 3 dimensions- Quantum confinement - energy subbands - Effective mass - Drude conduction - mean free path in 3D - ballistic conduction - phase coherence length - quantized conductance - Buttiker-Landauer formula- electron transport in pn junctions - short channel NanoTransistor –MOSFETs - Advanced MOSFETs - Trigate FETs, FinFETs - CMOS.

UNIT – III: Molecular NanoElectronics:

Electronic and optoelectronic properties of molecular materials - Electrodes & contacts – functions – molecular electronic devices - elementary circuits using organic molecules- Organic materials based rectifying diode switches – TFTs- OLEDs- OTFTs – logic switches.

UNIT – IV: Spintronics:

Spin tunneling devices - Magnetic tunnel junctions- Tunneling spin polarization - Giant tunneling using MgO tunnel barriers - Tunnel-based spin injectors - Spin injection and spin transport in hybrid nanostructures - spin filters -spin diodes - Magnetic tunnel transistor - Memory devices and sensors - ferroelectric random access memory- MRAMS -Field Sensors - Multiferro electric sensors- Spintronic Biosensors.

UNIT – V: NanoElectronic Architectures & Computations:

Architecture Principles: Mono and Multi processor systems – Parallel data processing – Power Dissipation and Parallelism – Classic systolic arrays - Molecular devices-properties - Self-organization – Size dependent -limitations. Computation: Monte Carlo Simulations- Computational methods and Simulations from ab initio to multiscale Modeling- Modeling of Nanodevices.

Text Books:

1. V. Mitin, V. Kochelap, M. Stroscio, “Introduction to Nanoelectronics,” Cambridge University Press, 2008.
2. Rainer Waser, “Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices,” Wiley-VCH, 2003.

References:

1. Karl Goser, Peter Glosekotter, Jan Dienstuhl, "Nanoelectronics and Nanosystems," Springer, 2004.
2. Sadamichi Maekawa, "Concepts in Spin Electronics," Oxford University Press, 2006.
3. L. Banyai and S.W.Koch, "Semiconductor Quantum Dots," World Scientific, 1993.
4. Edward L. Wolf, "Nanophysics and Nanotechnology: An Introduction to Modern Concepts in Nanoscience," Wiley-VCH, 2006.

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(15D41110) CMOS VLSI DESIGN

Course Objective:

- To study about MOS devices and their modelling
- To study CMOS inverter and its characteristics
- To study about realization of both combinational and sequential modules
- To study about different types of memories

Course Outcome:

After completion of the course the student will be able to

- Gain complete knowledge regarding MOS devices and their modelling.
- Know the working of CMOS inverter and various parameters that effects its performance
- Realize different combinational and sequential modules
- To get complete knowledge regarding Memories

UNIT-I:

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

MOS Design

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Sequential MOS Logic Circuits

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT -III:

Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Semiconductor Memories

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

UNIT -IV:

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-V:

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

Text Books:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", TMH, 3rd Ed., 2011.
3. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International Second Edition/Indian Edition, 2010.
4. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley India, Fifth Edition, 2010.

References:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition.
3. Baker, Li and Boyce, "CMOS: Circuit Design, Layout and Simulation", PHI.
4. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Ed., PHI.

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(15D42102) ADVANCED DIGITAL SIGNAL PROCESSING

Course Objective:

- To study about the digital signal processing algorithms and multi rate signal processing
- To study about the power spectral estimation by using Barlett, Welch & Blackmann & Tukey methods.
- The study about the effects of finite word length in fixed-point dsp systems..

Course Outcome:

After completion of the course students will be able to

- Get complete knowledge regarding various algorithms associated with Digital signal processing and multi rate signal processing.
- Verify the power spectral estimation by using Barlett, Welch & Blackmann & Tukey methods.
- Understand the effects of finite word length in fixed-point DSP systems by using ADC and FFT algorithms.

UNIT I

DSP ALGORITHEMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT II

MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT III

POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett, Welch & Blackmann & Tukey methods.

PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT IV

ANALYSIS OF FINITE WORDLENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality-Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT V

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Non stationary Signals, Musial Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete-Time Analytic Signal Generation.

Text Books:

1. Sanjit K Mitra, "Digital Signal Processing", Tata MCgraw Hill Publications.
2. J G Proakis, D G Manolokis, "Digital Signal Processing Principles, Algorithms, Applications" PHI.

References:

1. A V Oppenhiem, R W Schafer, "Discrete-Time Signal Processing", Pearson Education.
2. Emmanuel C Ifeacher Barrie. W. Jervis, "DSP- A Practical Approach", Pearson Education.
3. S. M .Kay, "Modern spectral Estimation Techniques" PHI, 1997

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M.Tech I Sem	**T**	**P**	**C**
	4	**0**	**4**

(15D41111) CLOUD COMPUTING

Course Outcomes : After completion of this subject, students will be able to

- Under stand the concepts of distributed systems, parallel computing, cluster computing and virtualization.
- Design and implement cloud networks for various applications.
- Maintain cloud data centers and cloud based information systems for cloud computing.

UNIT I:

Introductory concepts and overview: Distributed systems, Parallel computing architectures: Vector processing, Symmetric multi processing and Massively parallel processing systems, High performance Cluster computing, Grid computing, Service Oriented Architecture overview, Virtualization.

UNIT II:

Web services delivered from the cloud: Infrastructure as a service, Platform-as-a-service, Software-as-a-service. Building Cloud networks: Evolution from the MSP model to cloud computing and software-as-aservice, The cloud data center, SOA as step toward cloud computing, Basic approach to a data center based SOA.

UNIT III:

Federation Presence, Identity and Privacy in the cloud: Federation in the cloud, Presence in the cloud, Privacy and its relation to cloud based information system. Security in the Cloud: Cloud security challenges, Software-as-a-service security.

Common Standards in Cloud computing:The open cloud consortium, The distributed management task force, standards for application developers, standards for messaging, standards for security.

UNIT IV:

End user access to cloud computing: youtube, zimbra, Facebook, Zoho, DimDim Collaboration Mobile internet devices and the cloud: Smartphone, mobile operating systems for smart phones, Mobile Platform virtualization, Collaboration applications for mobile platforms, Future trends.

UNIT V:

Virtualization: Adding guest Operating system. Cloud computing case studies1: Amazon EC2, Amazon simple DB, Amazon S3, Amazon Cloud Front, Amazon SQS.

Text Books:

1. John W. Rittinghouse, James F. Ransome, “Cloud Computing implementation, management and security”, CRC Press, Taylor & Francis group, 2010.
2. Anthony T.velte, Toby J.velte Robert Elsenpeter “Cloud Computing: A practical approach”, Tata McGraw Hill edition, 2010.

References:

1. George Reese , “Cloud Application Architectures”, Oreilly publishers.
2. David S. Linthicum, Addison, “Cloud Computing and SOA convergence in your enterprise”, Wesley Publications.

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M.Tech I Sem	**T**	**P**	**C**
	0	**3**	**2**

(15D41112) STRUCTURAL DIGITAL SYSTEM DESIGN LAB

Course Objective:

- To understand about VHDL and Verilog Programming in all available styles.
- To understand differences between Verilog and VHDL.
- To represent the different digital blocks in verilog and VHDL in all available styles of modelling

Course Outcome:

After completion of this course the students will be able to understand

- Different modelling styles available in VHDL and Verilog and difference between them
- Difference between verilog and VHDL
- Representation of different digital modules in different modelling styles available in VHDL and Verilog

Using VHDL and Verilog do the following experiments

1. Design of 4-bit adder / subtractor
2. Design of Booth Multiplier
3. Design of 4-bit ALU
4. Design 32-bit ALU using ripple carry and carry look-ahead logic
5. Design of counters and shift registers
6. Design of MIPS processor
7. Design of Washing machine controller
8. Design of Traffic Light Controller
9. Mini project

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(15D41201) EMBEDDED SYSTEM DESIGN

Course Objective:

- To study about current technologies, integration methods and hardware and software design concepts associated with processor in Embedded Systems.
- To study about a simple low power microcontrollers and their applications
- To get detail knowledge regarding testing and hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers

Course Outcome:

After completion of this course the students will be able to understand

- The issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- The concept of low power microcontrollers.
- The hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers.

UNIT – I

Introductionto Embedded Electronic Systems and Microcontrollers:

An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware:The Embedded Board and the von Neumann Model, Embedded Processors: ISAArchitectureModels, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430).

UNIT-II

MSP430 – I:

Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.

Functions, Interrupts, and Low-Power Mode: Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

UNIT – III

MSP430 – II:

Digital Input, Output, and Displays: Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

Timers: Watchdog Timer, Timer_A, Timer_A Modes, Timer_B,Timer_B Modes, Setting the Real-Time Clock, State Machines.

UNIT – IV

MSP430 Communication:

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, AThermometer Using SPI Modes,Inter-integrated Circuit Bus(I^2C) and its operations, State Machines for I^2C Communication, AThermometer Using I^2C, Asynchronous Serial Communication, Asynchronous Communication with the USCI_A, ASoftware UART Using Timer_A, Other Types of Communication.

UNIT – V

MSP430 Case Studies:

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I^2C.

Text Books:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
2. John H. Davies "MSP430 Microcontroller Basics",Elsevier Ltd Publications, Copyright 2008.

References:

1. Manuel Jiménez Rogelio,PalomeraIsidoroCouvertier "Introduction to Embedded SystemsUsing Microcontrollers and the MSP430" Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.
3. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
4. Arnold S Burger, "Embedded System Design", CMP Books, 2002.
5. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications,Second Edition, 2008.

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(15D41202) IMAGE AND VIDEO PROCESSING

Course Objective:

- To understand different transforms related to gray scale and color images.
- To get complete knowledge regarding different techniques associated with Image Enhancement, Image Restoration, Image Segmentation and Image Compression.
- To get clear knowledge regarding motion estimation, video filtering and video standards

Course Outcome:

After completion of this course the students will be able to

- Different transforms related to gray scale and color images.
- Complete knowledge regarding different techniques associated with Image Enhancement, Image Restoration, Image Segmentation and Image Compression.
- Understand basic concepts regarding to motion estimation, video filtering and video standards.

UNIT I

IMAGE FUNDAMENTALS & TRANSFORMS: Gray scale and color Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge detection, non parametric and model based approaches, LOG filters, localization problem.

IMAGE RESTORATION: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT III

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Edge detection, Hough transform, Region growing.

UNIT IV

IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem. Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT V

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation. Video Filtering, Video Compression, Video coding standards.

References:

1. R. C. Gonzalez, R. E. Woods,"Digital Image Processing", Pearson Education. 2nd edition,2002
2. W. K. Pratt, "Digital image processing", Prentice Hall, 1989

3. Rosenfold and A. C. Kak, “Digital image processing”, Vols. 1 and 2, Prentice Hall, 1986.
4. H. C. Andrew and B. R. Hunt, “Digital image restoration”, Prentice Hall, 1977
5. R. Jain, R. Kasturi and B.G. Schunck, “Machine Vision”, McGraw-Hill International Edition, 1995
6. M. Tekalp, “Digital Video Processing”, Prentice-Hall, 1995
7. Bovik, “Handbook of Image & Video Processing”, Academic Press, 2000

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(15D41203) ADSP ARCHITECTURES

Course Objective:

- To understand the concept of DSP Architecture & comparison of this with conventional microprocessors architecture.
- To understand addressing modes, instruction sets , pipelining and application programs in TMS320C54XX processor
- To understand the architectural issues of programmable DSP devices and their relationship to the algorithmic requirements, architectures of commercially popular programmable devices and the use of such devices for software development and system design
- To highlight the suitability of programmable DSP devices for various application areas and motivate to design systems around these devices.

Course Outcome:

- To become familiar with fundamentals of DSP Processors & architectures.
- To gain in knowledge about the different types of processors and their operation.
- Will demonstrate the ability to design a system component or process as per needs & specifications.
- Will demonstrate the ability to identify, formulate & solve engineering problems.

UNIT-I

Review of DSP – DFT and FFT, Correlation and convolution, FIR and IIR filter Design, Multirate Signal Processing, Hardware Implementation Approaches and Challenges, Assignment

UNIT-II

Computational Accuracy of DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP Implementations, AD/ DA conversion and DSP computational errors.

UNIT-III

Architectures for DSP Programmable Devices Basic architectural features, DSP computational building blocks: multiplier, Barrel Shifter, MAC, ALU; Bus architectures, On-chip organization, Address generation unit, Program control , Speed issues: Hardware architecture, Parallelism, Pipelining, System Level Parallelism and Pipelining

UNIT-IV

Programmable DSPs: TMS 320C54xx architecture, Data addressing modes, Memory space and program control, Instructions and programming, On-chip peripherals, Interrupts.

UNIT- V

FPGAs: Basics, Architectural features of modern FPGAs (Stratix/ Virtex), On-chip features , LPMs and Cores.

Text Books:

1. Avatar Singh and S. Srinivasan, “DSP Implementations using DSP Microprocessors”, Thomson Brooks/Cole - 2004

2. Uwe Meyer – Baese, "Digital Signal Processing with FPGAs", Springer, 2000
3. Navabi, Z., "Embedded Core Design with FPGAs", TMH – 2008

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(15D41204) ASIC DESIGN

Course Objective:

- To study different types of ASICs and their libraries.
- To study in detail about programmable Asics, I/O modules and their interconnects.
- To study about different methods of software ASIC design their simulation, testing and construction of ASICs.

Course Outcome:

After completion of the course the student will be able to

- Understand different types of ASICs and their libraries.
- Understands about programmable Asics, I/O modules and their interconnects.
- Gets complete knowledge regarding different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT I

INTRODUCTION TO ASICs:

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT II

PROGRAMABLE ASICS AND PROGRAMABLE ASIC LOGIC CELLS

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III

I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT IV

LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Senthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT V

SIMULATION, TEST AND ASIC CONSTRUCTION

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in

Self Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

References:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J.Herbst, "Intigrated Circuit Engineering", Oxford Science Publications, 1996.
3. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design compiler", 2nd Edition, Kluwer Academic, 2001.

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(15D41205) LOW POWER VLSI DESIGN

Course Outcomes : After completion of this subject, students will be able to

- Under stand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry LookAhead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, BaughWooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Text Books:

1.CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

References:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.

2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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(15D41206) CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Course Objective:

- To study about different types of Programmable Logic Devices.
- To Study in detail about the functioning, organization and specialized components associated with FPGAs
- To get complete knowledge pertaining to different FPGA Architectures and some design applications.

Course Outcome:

After completion of this course the students will be able to

- Understand functioning of different types of Programmable Logic Devices.
- Gets clear idea regarding functioning, organization and specialized components associated with FPGAs.
- Complete knowledge pertaining to different FPGA Architectures and some design applications.

UNIT-I: Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT-III: SRAM Programmable FPGAs

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT-IV: Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT-V: Design Applications

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

References:

1. Stephen M. Trimberger, “Field Programmable Gate Array Technology”, Springer International Edition.
2. Charles H. Roth Jr, “Digital Systems Design”, Lizy Kurian John, Cengage Learning.
3. John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
4. Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition.
5. Ian Grout, “Digital Systems Design with FPGAs and CPLDs”, Elsevier, Newnes.
6. Wayne Wolf, “FPGA based System Design”, Prentice Hall Modern Semiconductor Design Series.

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M.Tech II Sem	T	P	C
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(15D41207) HARDWARE SOFTWARE CO-DESIGN

Course Objective:

- To study about different issues and algorithms related to Co-Design and Co-Synthesis.
- To study about different techniques associated with Prototyping and Emulation.
- To get clear knowledge regarding Compilation Techniques, Tools, and different languages for associated with software and hardware co-design.

Course Outcome:

After completion of this course the students will be able to

- Understand different issues and algorithms related to Co-Design and Co-Synthesis.
- Study different techniques associated with Prototyping and Emulation.
- Complete knowledge regarding Compilation Techniques, Tools, and different languages for associated with software and hardware co-design.

UNIT-I:

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System – Level Specification and Design-I:

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

References:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / Software Co- Design Principles and Practice”, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware / Software Co- Design”, 2002, Kluwer Academic Publishers.
3. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design”, Springer Publications, 2010.
4. Ralf Niemann, “Hardware/Software Co-Design for Data flow dominated Embedded Systems ”, Kluwer Academic Publishers.
5. Joris Vanden Hurk, Jochen jess, “System Level Hardware/Software Co-Design”, Kluwer Academic Publishers.

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(15D41208) BIG DATA

Course Outcomes : After completion of this subject, students will be able to

- Understand the concepts of RDMS, Grid computing and Big data technologies.
- Maintain and manage big data bases for various applications
- Utilize Hadoop related tools for implementation of different data models and formats.

UNIT I:

UNDERSTANDING BIG DATA

What is big data – why big data –.Data!, Data Storage and Analysis, Comparison with Other Systems, Rational Database Management System , Grid Computing, Volunteer Computing, convergence of key trends – unstructured data – industry examples of big data – web analytics – big data and marketing – fraud and big data – risk and big data – credit risk management – big data and algorithmic trading – big data and healthcare – big data in medicine – advertising and big data – big data technologies – introduction to Hadoop – open source technologies – cloud and big data – mobile business intelligence – Crowd sourcing analytics – inter and trans firewall analytics

UNIT II:

NOSQL DATA MANAGEMENT

Introduction to NoSQL – aggregate data models – aggregates – key-value and document data models – relationships – graph databases – schema less databases – materialized views – distribution models – sharding — version – Map reduce – partitioning and combining – composing map-reduce calculations .

UNIT III:

BASICS OF HADOOP

Data format – analyzing data with Hadoop – scaling out – Hadoop streaming – Hadoop pipes – design of Hadoop distributed file system (HDFS) – HDFS concepts – Java interface – data flow – Hadoop I/O – data integrity – compression – serialization – Avro – file-based data structures

UNIT IV:

MAPREDUCE APPLICATIONS

MapReduce workflows – unit tests with MRUnit – test data and local tests – anatomy of MapReduce job run – classic Map-reduce – YARN – failures in classic Map-reduce and YARN – job scheduling – shuffle and sort – task execution – MapReduce types – input formats – output formats

UNIT V:

HADOOP RELATED TOOLS

Hbase – data model and implementations – Hbase clients – Hbase examples –praxis. Cassandra – Cassandra data model – cassandra examples – cassandra clients –Hadoop integration. Pig – Grunt – pig data model – Pig Latin – developing and testing Pig Latin

scripts. Hive – data types and file formats – HiveQL data definition – HiveQL data manipulation – HiveQL queries.

Text Books:

1. Tom White, "Hadoop: The Definitive Guide", Third Edition, O'Reilley, 2012.
2. Eric Sammer, "Hadoop Operations", O'Reilley, 2012.

References:

1.VigneshPrajapati, Big data analytics with R and Hadoop, SPD 2013.
2. E. Capriolo, D. Wampler, and J. Rutherglen, "Programming Hive", O'Reilley, 2012.
3. Lars George, "HBase: The Definitive Guide", O'Reilley, 2011.
4. Alan Gates, "Programming Pig", O'Reilley, 2011.

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(15D41209) FUZZY SYSTEMS AND NEURAL NETWORKS

Course Objective:

- To analyze basic neural computational models.
- To get in detail knowledge regarding different algorithms related to neural learning
- To study about different issues related probability and fuzziness and different types of fuzzy associative memories.

Course Outcome:

After completion of this course the students will be able to

- Understand functioning of basic neural computational models.
- Get complete knowledge regarding different algorithms related to neural learning
- Understand about different issues related probability and fuzziness and different types of fuzzy associative memories.

UNIT-I

INTRODUCTION: History of Neural Networks, Structure and functions of biological and artificial neuron, Neural network architectures, learning methods, evaluation of neural networks. McCulloch- Pitts neuron model, perception learning, Delta learning, Windrow-Hoff learning rules, linear seperability, Adaline, Modifications.

UNIT - II

SUPERVISED LEARNING: Architectures, Madalines, Back propagation algorithm, importance of learning parameter and momentum term, radial basis functions.

UNSUPERVISED LEARNING : Winner – Take – all learning, out star learning, learning vector quantizers, Counter propagation networks, Kohonen self – organizing networks, Grossberg layer, adaptive resonance theory, Hamming net.

UNIT – III

ASSOCIATIVE MEMORIES: Hebbian learning rule, continues and discrete Hopfild networks, recurrent and associative memory, Boltzman machines, Bi-directional associative memory

UNIT-IV

FUZZINESS VS PROBABILITY: Fuzzy Sets & Systems; The Geometry of Fuzzy sets; The Fuzzy Entropy Theorem; The Subsethood Theorem; The Entropy Subsethood Theorem.

UNIT - V

FUZZY ASSOCIATIVE MEMORIES: Fuzzy & Neural Function Estimators; Fuzzy Hebbian FAMs; Adaptive FAMs.

References:

1. J.M. Zurada, “Introduction to Artificial Neural Systems” - Jaico Publishing House, Bombay,2001.
2. Kishan Mehrotra , Chelkuri. K.Mohan, Sanjay Ranka, “Elements of Artificial Neural Networks”, Penram International
3. S.N Sivanandham, S. sumathi, S.N.Deepa,“Introduction to Neural networks using matlab 6.0”, Tata McGraw Hill, New Delhi, 2005.
4. B.Kosko, “Neural Networks & Fuzzy Systems”, Prentice Hall (India) Ltd., 1992.

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(15D41210) MEMS AND ITS APPLICATIONS

Course Objective:

- To study about fabrication processes involved in different types of sensors.
- To Study about characteristics of different MEMS materials.
- To get complete knowledge regarding working of MEMS Switches, relays, Inductors, Capacitors and Packing techniques associated with MEMS.

Course Outcome:

After completion of this course the students will be able to

- Understand different steps involved in fabrication processes of different types of sensors.
- Understand characteristics of different MEMS materials.
- Get complete knowledge regarding working of MEMS Switches, relays, Inductors, Capacitors and Packing techniques associated with MEMS.

UNIT-I:

MEMS Fabrication processes & Sensors*:*

Introduction, MEMS Overview, Micro-fabrication of MEMS: Surface Micromachining, Bulk Micromachining, LIGA, micromachining of polymeric MEMS devices, Three-dimensional micro-fabrications. Electromechanical transducers: Piezoelectric transducers, Electro-strictive transducers, Magneto-strictive transducers, Electrostatic actuators, Electromagnetic transducers, Electro-dynamic transducers, Electro-thermal actuators, comparison of electro-thermal actuation process, Micro-sensing for MEMS: Piezo-resistive sensing, Capacitive sensing, Piezoelectric sensing, Resonant sensing, Surface Acoustic Wave sensors.

UNIT-II:

MEMS Materials and Fabrication techniques: Metals, semiconductors, thin films for MEMS and their deposition techniques, materials for polymer MEMS, Bulk micromachining for silicon based MEMS, Silicon surface micromachining, Micro-stereo-lithography for polymer MEMS.

UNIT-III:

MEMS Switches and Micro relays: Switch parameters, basics of switching, Switches for RF and microwave applications, actuation mechanisms for MEMS devices, bistable micro relays and micro-actuators, dynamics of switch operation, MEMS switch design considerations, modeling and evaluation.

UNIT- IV:

MEMS Inductors and Capacitors: MEMS Micro-machined passive elements: pros and cons, MEMS Inductors: self and mutual inductance, micro-machined inductors, reduction of stray capacitance, improvement of quality factor, folded inductors, modeling and design issues of planar inductors, variable inductor and polymer based inductor. MEMS Capacitors: MEMS gap tuning capacitor, MEMS area tuning capacitor, Dielectric Tunable capacitors.

UNIT-V:

MEMS packaging & MEMS RF Applications: MEMS packaging: Role of MEMS packaging, Types of MEMS packaging, flip-chip and multichip Unit packaging, RF MEMS packaging issues. MEMS RF applications: Micro-machined transmission line and components, micro-machined RF Filters, Micro-machined Phase shifters, and Micro-machined antenna, Gyros and Bio-MEMS.

References:

1. Gabriel M. Rebeiz, "RF MEMS: Theory, Design, and Technology," John Wiley & Sons, 2003.
2. Vijay K. Varadan, K. J. Vinoy and K. A. Jose, "RF MEMS & Their Applications," John Wiley & Sons, 2003.
3. Tai-Ran Hsu, "MEMS and Microsystems: Design and Manufacture," McGraw- Hill.

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M.Tech II Sem	**T**	**P**	**C**
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(15D41211) TESTING AND TESTABILITY

Course Objective:

- To Study about different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits.
- To study in detail about different methods of simulation and algorithms associated with testing.
- To get clear knowledge regarding working BIST, different parameter and techniques associated with BIST.

Course Outcome:

After completion of this course the students will be able to

- Understand different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits.
- Study about different methods of simulation and algorithms associated with testing.
- Get complete knowledge about different methods of simulation and algorithms associated with testing.

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

References:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
3. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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M.Tech II Sem	**T**	**P**	**C**
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(15D41212) WIRELESS SENSOR NETWORKS

Course Objective:

- To study about different types of sensor networks, advantages, applications and the mechanism of transportation and processing involved in Wireless Sensor Networks.
- To study about representation and different protocols and mechanisms involved in routing of Wireless Sensor Networks.
- To study about tools and simulators associated with Wireless Sensor Networks.

Course Outcome:

After completion of this course the students will be able to

- Understand different types of sensor networks, advantages, applications and the mechanism of transportation and processing involved in Wireless Sensor Networks.
- Understand about representation and different protocols and mechanisms involved in routing of Wireless Sensor Networks.
- Gets complete knowledge regarding different tools and simulators associated with Wireless Sensor Networks.

UNIT-I

Sensor networks, advantages and applications, Sensor Network Applications - Habitat Monitoring, Smart Transportation, Collaborative Processing

UNIT - II

Localization and tracking,- sensing model, Distributed Representation, Tracking Multiple Objects networking sensors- Medium Access Control, *Energy-Aware Routing to a Region,* Attribute-Based Routing

UNIT-III

Infrastructure Establishment -Clustering and time synchronizations, Localization and localization services, Sensor tracking and control - Task-Driven Sensing, Information-Based Sensor Tasking, Sensor Group Management

UNIT-IV

Sensor Network data bases - Sensor Database Challenges , Query Interfaces , Data-Centric Storage, Multidimensional Indices for Orthogonal Range Searching, Locality-Preserving Hashing

UNIT - V

Sensor Network Platforms and Tools -Sensor Network hardware, Node level software, Node-Level Simulators, wireless sensor networks positioning and location management.

References:

1. F. Zhao, C Guibas, “Wireless Sensor Networks”, Elsevier, Morgan Kaufmann, 2004.
2. Kazem Sohraby, Daniel Minoli, Taieb Znati, “Wireless Sensor Networks -Technology, Protocols and Applications”, John Wiley & Sons, 2007.

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(15D54201) RESEARCH METHODOLOGY
(Audit Course)

UNIT I

Meaning of Research – Objectives of Research – Types of Research – Research Approaches – Guidelines for Selecting and Defining a Research Problem – research Design – Concepts related to Research Design – Basic Principles of Experimental Design.

UNIT II

Sampling Design – steps in Sampling Design –Characteristics of a Good Sample Design – Random Sampling Design.

Measurement and Scaling Techniques-Errors in Measurement – Tests of Sound Measurement – Scaling and Scale Construction Techniques – Time Series Analysis – Interpolation and Extrapolation.

Data Collection Methods – Primary Data – Secondary data – Questionnaire Survey and Interviews.

UNIT III

Correlation and Regression Analysis – Method of Least Squares – Regression vs Correlation – Correlation vs Determination – Types of Correlations and Their Applications

UNIT IV

Statistical Inference: Tests of Hypothesis – Parametric vs Non-parametric Tests – Hypothesis Testing Procedure – Sampling Theory – Sampling Distribution – Chi-square Test – Analysis of variance and Co-variance – Multi-variate Analysis.

UNIT V

Report Writing and Professional Ethics: Interpretation of Data – Report Writing – Layout of a Research Paper – Techniques of Interpretation- Making Scientific Presentations in Conferences and Seminars – Professional Ethics in Research.

Text books:

1. Research Methodology:Methods and Techniques – C.R.Kothari, 2nd Edition,New Age International Publishers.
2. Research Methodology: A Step by Step Guide for Beginners- Ranjit Kumar, Sage Publications (Available as pdf on internet)
3. Research Methodology and Statistical Tools – P.Narayana Reddy and G.V.R.K.Acharyulu, 1st Edition,Excel Books,New Delhi.

References:

1. Scientists must Write - Robert Barrass (Available as pdf on internet)
2. Crafting Your Research Future –Charles X. Ling and Quiang Yang (Available as pdf on internet)

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M.Tech II Sem	**T**	**P**	**C**
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(15D41213) EMBEDDED SYSTEM DESIGN LAB

Course Outcomes:

After Completion of this Lab, Students will be able to

- Design and Implement basic circuits that are used in Embedded systwms.
- Develop code using appropriate tools.
- Test the circuit performance with standard benchmark circuits.

List of Experiments:

Note. Any Ten Experiments from the following (Experiment – 1 is mandatory)

1. A Study of Code Composer Studio (CC Studio Latest Version)
2. Flashing a light by a software delay.
3. Displaying Characters on LCD.
4. Serial Communication using UART.
5. Basic Input and Output using MSP430 UART.
6. Interrupt Handling using MSP430.
7. Analog to Digital Conversion using MSP430.
8. Interfacing external Devices to GPIO Ports
9. Simple Hexadecimal Calculator.
10. Flashing Lights by Polling timers
11. Subroutine calls using MSP430.
12. GPIO Using Interrupt handling using timers